LOW POWER TECHNIQUES OVERVIEW – FOR SOC

Master 2 – SETI | Paris-Saclay University

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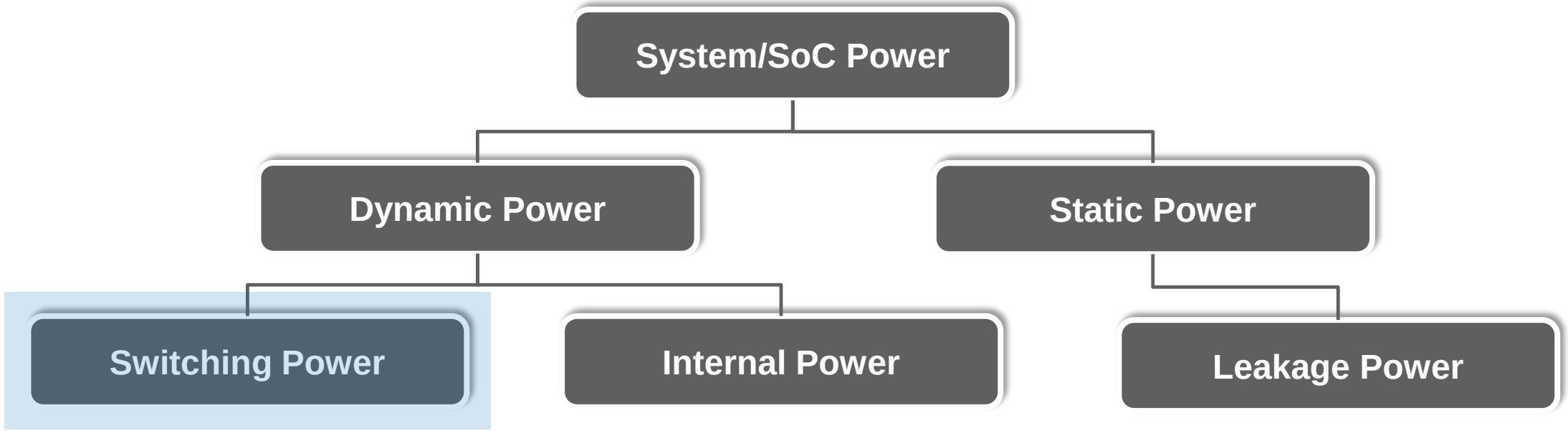
POWER OVERVIEW – SYSTEM/SOC



System Power = Dynamic Power + Static Power

Note: *Static Power part is not important compared to Dynamic Power part.*

POWER OVERVIEW : DYNAMIC POWER – SWITCHING PART

- Power generated due to output/signal changes, thus charging and discharging the load capacitance.

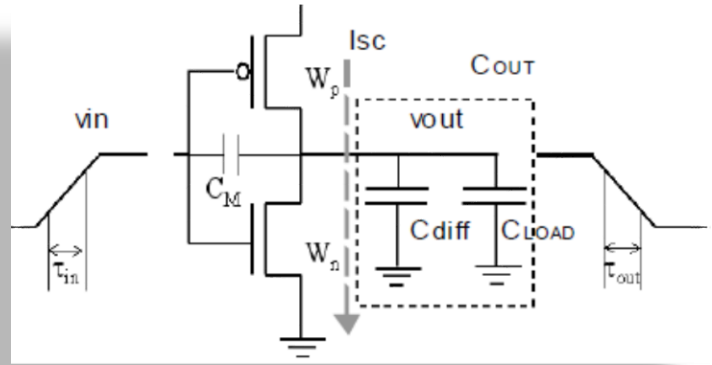
- Switching power dissipates mainly depend on the :
  - System **Clock Frequency**
  - **Activity Switching** Frequency

- Switching Power Calculation depends on the three factors
  - $C - Load\ Capacitance$
  - $f - Switching\ Freqency$
  - $V - Voltage$

$$P_S = C * V^2 * f$$

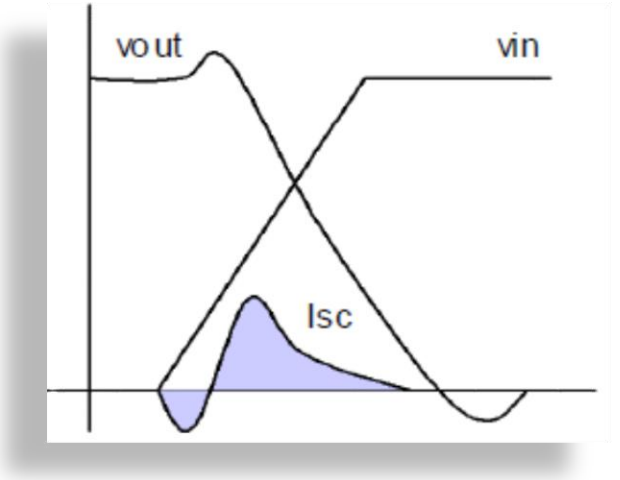
POWER OVERVIEW : DYNAMIC POWER – INTERNAL PART

- **Short circuit path** has been created between **power** and **ground** at the transition stage



- Thus the **short circuit current** is generated

- **Power dissipation** due to this temporary short circuit path and the internal capacitance is **Internal Power**



- Depends on some factors,
  - Input edge time
  - Slew Rate
  - Internal Capacitances

$$P_I = V * I_{SC}$$

DYNAMIC POWER

- **Dynamic power** is the sum of **switching power** and **internal power**

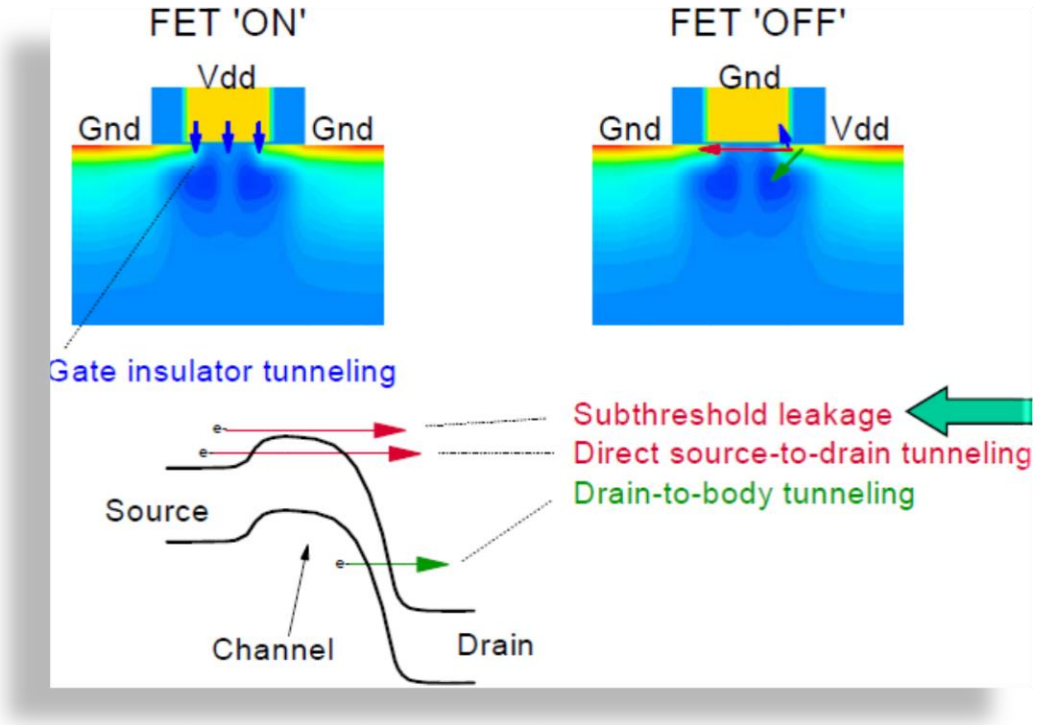
$$P_D = P_S + P_I$$

$$P_D = C * V^2 * f + V * I_{SC}$$

$$\boldsymbol{P_D \doteq C_{eff} * V^2 * f_{switch}}$$

STATIC POWER

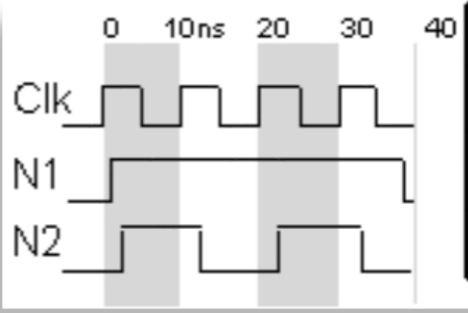
- Due to **non-idle characteristic** of the transistor the leakages can be taken place
- **Static power** is nothing, but **leakage power**
- There are two main types of leakages and their subsidiaries
  - I_{OFF} – Sub-threshold leakage (Drain Leakage Current)
    - $I_{D,weak} - Sub - threshold\ Drain\ Current$
    - $I_{inv} - Reverse\ Biased\ Current$
    - $I_{GIDL} - Gate\ Induced\ Drain\ Leakage$
  - I_{GATE} – Gate Leakage Current
    - $I_{TUNNEL} - Gate\ Tunneling$
    - $I_{HC} - Hot\ Carrier\ Injection$



POWER ESTIMATION

- Mostly based on the **tech libraries**

- Based on two major calculations
  - **Activity**
    - The number of toggles per clock cycle on the signal, averaged over many cycles
  - **Probability**, and **Percentage** of the time that the signal will be high



Activity	Probability
2.0	0.5
0.5	0.9
1.0	0.5

$$P = \frac{\text{(time at logic 1)}}{\text{total time}}$$

Clock cycle boundaries do not matter

LOW POWER TECHNIQUES

- DVFS – Dynamic Voltage Frequency Scaling
- DPM, Clock Gating, Power Gating
- Multi VDD, Voltage Islands
- Device Level
  - Multi Threshold Devices
  - Low Capacitance in device
  - High k Hf based MOS

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LOW POWER TECHNIQUES : DVFS - DYNAMIC VOLTAGE AND FREQUENCY SCALING (1/3)

- DVFS is a method to provide variable **amount of energy** for a task by **scaling** the **operating voltage/frequency**.

- Power consumption of a CMOS-based circuit is :

$$P_D \hat{=} \alpha * C_{eff} * V^2 * f$$

α : switching factor
C_{eff} : effective capacitance
V : operating voltage
f : operating frequency

- **Energy** required to run a task during T is :

$$E = P \cdot T \propto V2$$

(assuming $V \propto f$, $T \propto f^{-1}$)

- By **lowering** CPU frequency, CPU energy can be saved.

LOW POWER TECHNIQUES : DVFS - DYNAMIC VOLTAGE AND FREQUENCY SCALING (2/3)

Choosing a frequency in DVFS

- Workload of a task, W_{task}, is defined as the **total number** of **CPU clock cycles** required to finish the task :

$$W_{task} \equiv \sum_{i=1}^{N} CPI_i$$

N : total number of instructions in a task
CPI : clock cycles per instruction

- Task execution time, T_{task}, is a function of the CPU frequency, f^{cpu}

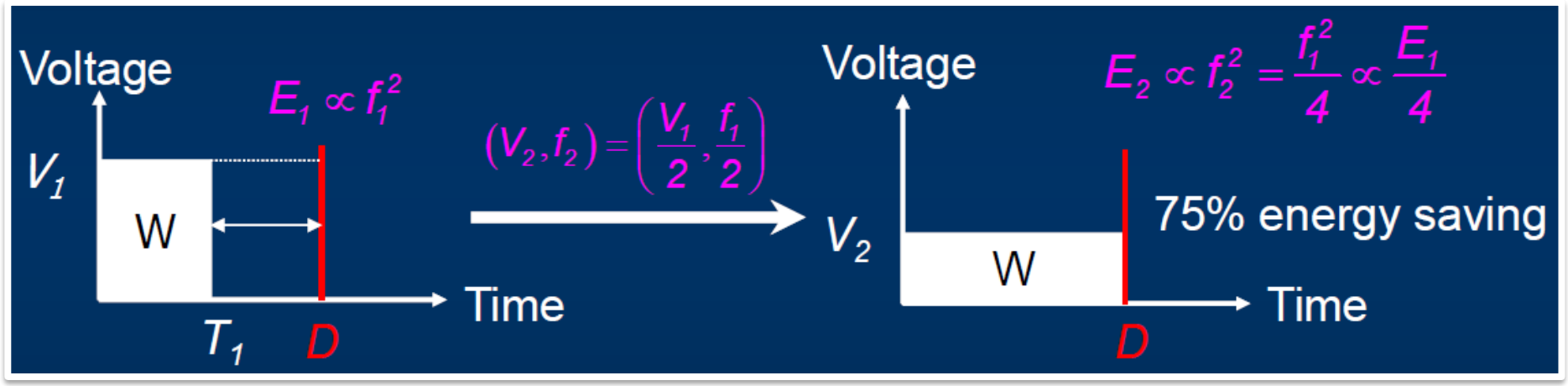
$$T_{task} = \frac{W_{task}}{f^{cpu}}$$

- Given a deadline of D, f_{target} denotes the CPU frequency that results in T_{task} closest to D

$$f_{target} = \frac{W_{task}}{D} \Rightarrow T_{task} = D$$

LOW POWER TECHNIQUES : DVFS - DYNAMIC VOLTAGE AND FREQUENCY SCALING (3/3)

- Example : a task with workload *W* should be completed by a deadline, *D*.



- DVFS is an effective way of reducing the CPU energy consumption by providing **"just-enough"** computation power.

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LOW POWER TECHNIQUES : DPM, CLOCK GATING, POWER GATING (1/5)

- **Clock Circuitry** Power Consumption
  - 15 to 45% of **Total Power**
  - P (clock circuitry) ∝ Frequency

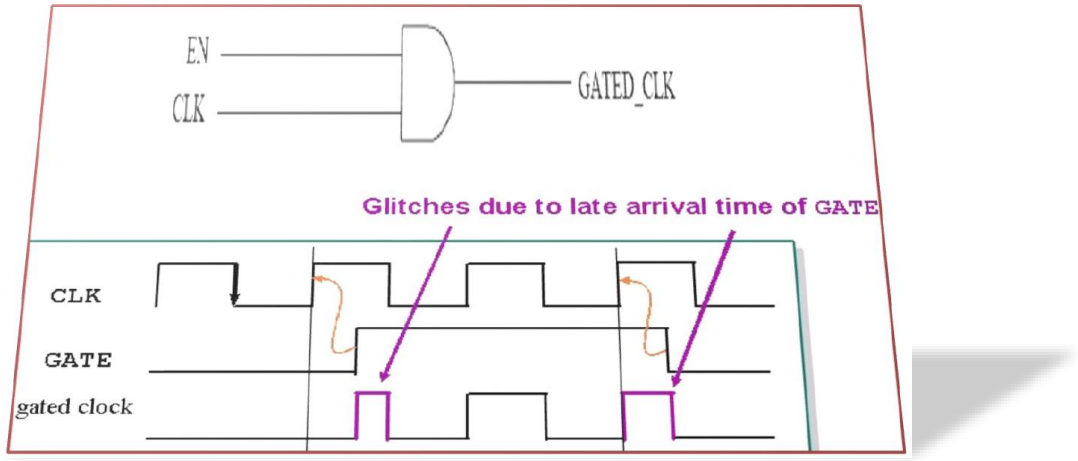
- **Clock tree** consume more than 50 % of **dynamic power**. The components of this power are:
  - Power consumed by **combinatorial logic** whose values are changing on each clock edge, and
  - Power consumed by **flip-flops**

- Activity of Functional Units
  - A (units) < 50% in Execution Time

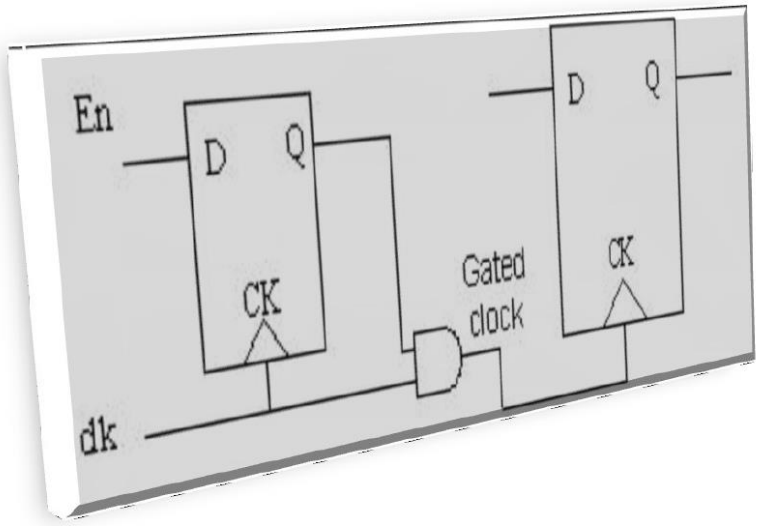
LOW POWER TECHNIQUES : DPM, CLOCK GATING, POWER GATING (2/5)

- Clock Gating and Power Reduction : two types :
  a. Latch-free clock gating
  b. Latch-based clock gating

(a)



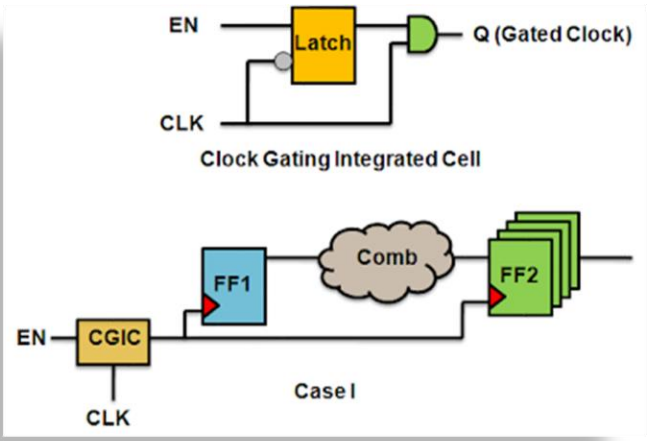
(b)



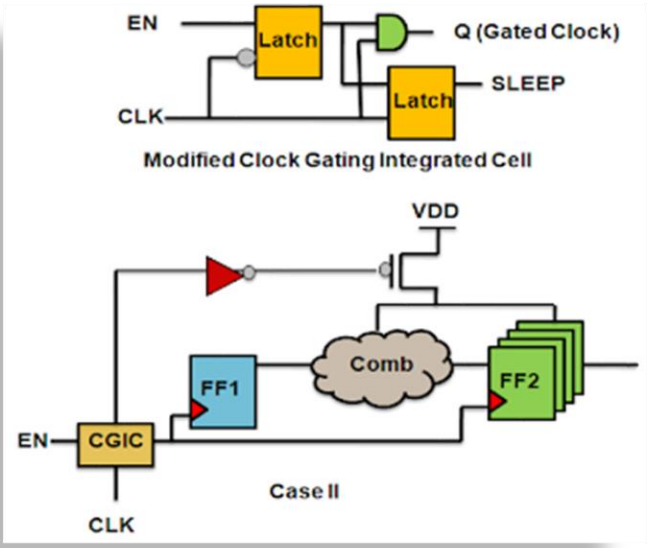
LOW POWER TECHNIQUES : DPM, CLOCK GATING, POWER GATING (3/5)

- Clock Main Idea
  - Clock Circuitry Gating (Case I)
  - Shutting/Power down Unused Partitions (Case II)
- Implementation
  - Creating Local Clocks
  - Buffers or Flip-Flops with **enable** or/and **Sleep** signal
- Net Effects
  - Reduction of Unnecessary Switching
    - Reduction of Clock Circuitry
  - Power Consumption Reduction

Only Clock Gating



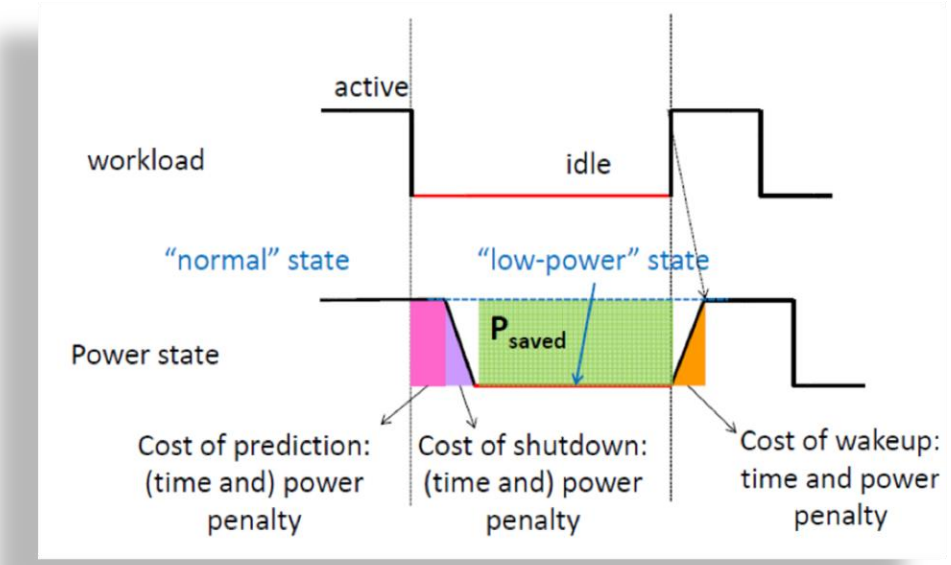
Clock & Power Gating



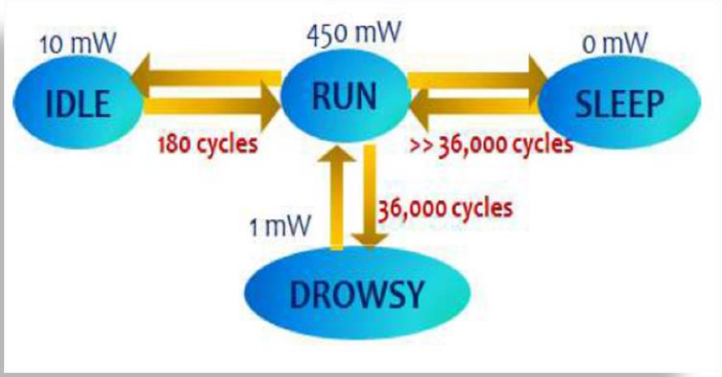
LOW POWER TECHNIQUES : DPM, CLOCK GATING, POWER GATING (4/5)

- Dynamic Power Management Main Idea
  - **Active the good power mode** of each system component
  - Shutting/Idle/Sleep down unused components
- Implementation
  - Inactivity period **prediction** and/or **calculation** depending in workload
  - **Optimal power states** definition and activation
- Component Effects
  - **Power down** unused/inactive components
  - Power Consumption Reduction

Power Saved

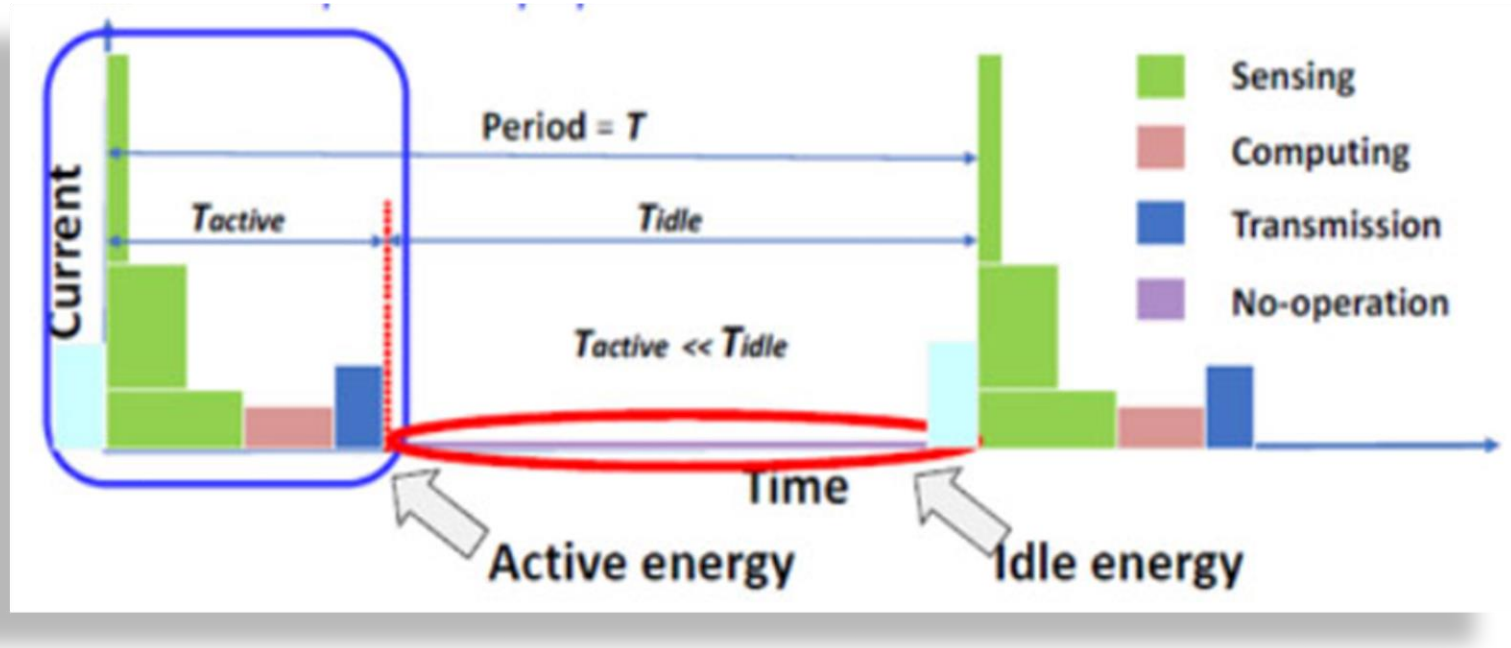


Power State Machine (PSM)



LOW POWER TECHNIQUES : DPM, CLOCK GATING, POWER GATING (5/5)

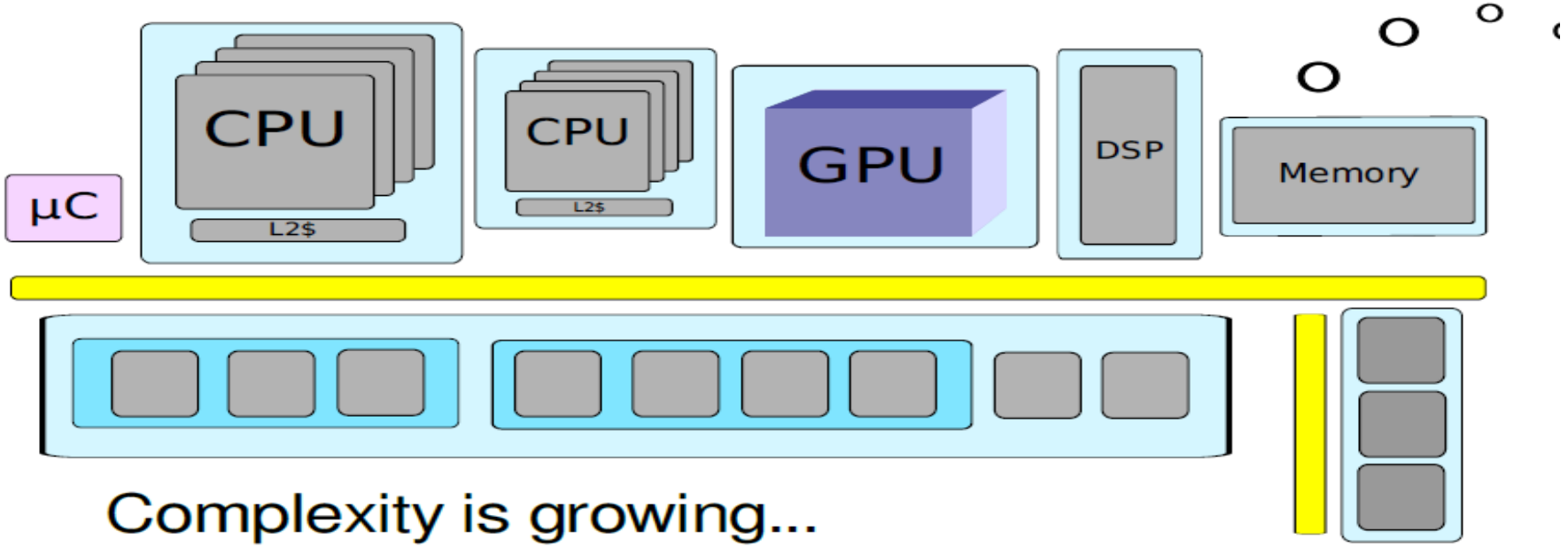
IoT : Sensors Nodes power saving example



- Component Effects
  - Power down unused/inactive components
  - Power Consumption Reduction

Architecture

LOW POWER TECHNIQUES : RUNTIME SUPPORT (1/2)

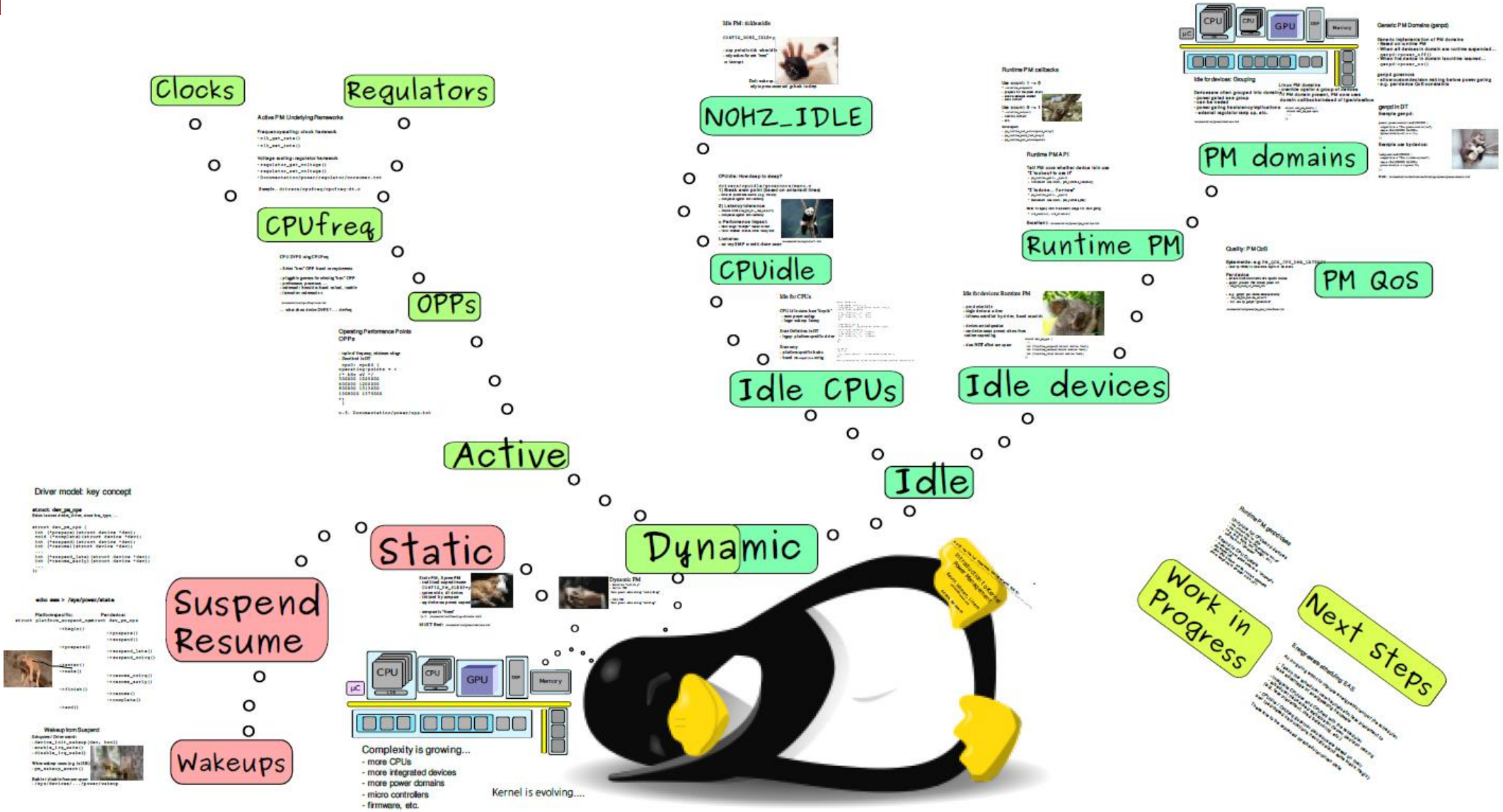


Complexity is growing...
- more CPUs
- more integrated devices
- more power domains
- micro controllers
- firmware, etc.

Kernel is evolving....

To support several power management techniques

LOW POWER TECHNIQUES : RUNTIME SUPPORT (2/2)



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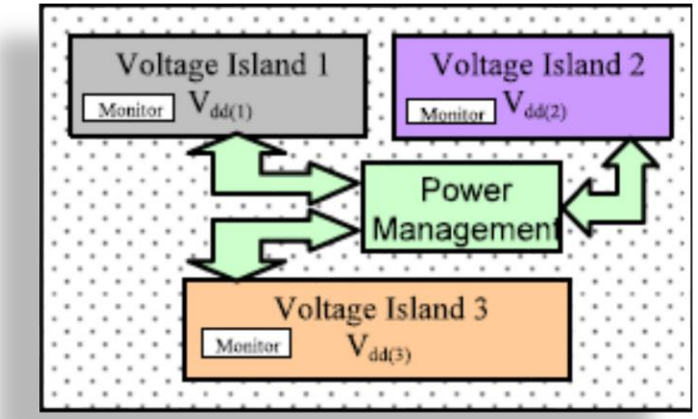
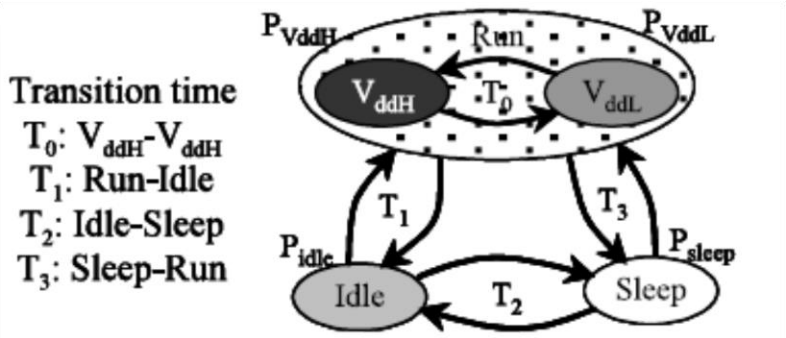
LOW POWER TECHNIQUES : MULTI VDD, VOLTAGE ISLAND

- Multi-VDD design Main Idea
  - Allows a finite number of supply voltages depending on power requirements of the system.
  - Dynamic change of voltage supply depending on the workload
- Implementation
  - Multi-VDD design sectors
  - Advanced optimal power states definition and activation
- Component Effects
  - Fine Grain Power management
  - Power Consumption Reduction

Multiple Voltage Island Design



Power State Machine (PSM) with Multi-VDD



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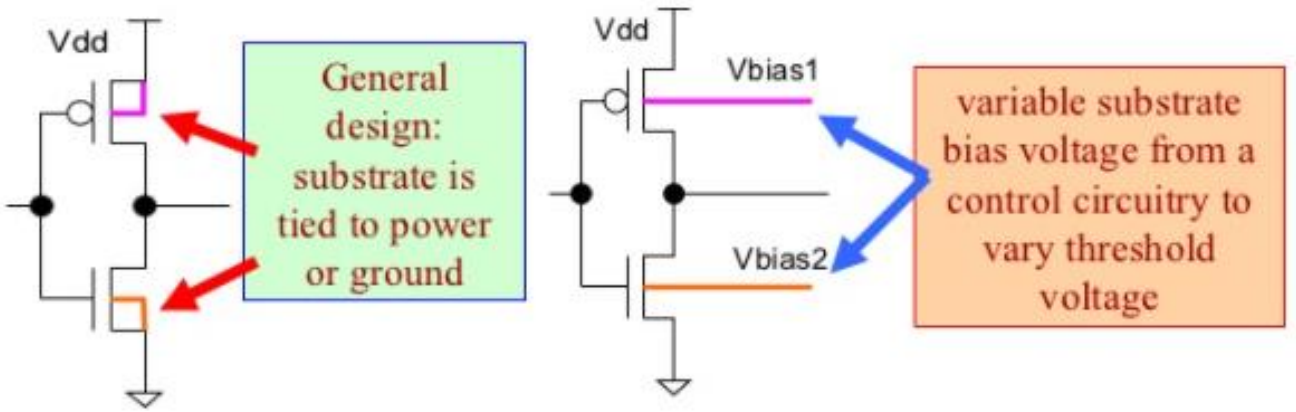
LOW POWER TECHNIQUES : MULTI-THRESHOLD DEVICES (CMOS)

- Multi-threshold is one kind of CMOS which is a deviation in the chip technology.
  - It has transistor with **multiple threshold voltages** in order to optimize delay or power.
  - It can achieve a **lower threshold voltage**, and therefore, **higher performance** as well as **smaller** standby leakage current.
  - Simple threshold of making MOS with **multiple threshold voltages** is to apply **different bias voltage** to the body or substrate terminal of the transistors.
  - It enables **high performance** and **low power operation**, but requires sequential circuit structures that can retain state during standby modes.



Thank you

Any Question ?

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